REMARKS

The following is in response to the Office Action mailed on July 1, 2005. The Office Action rejected claims 40-54 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. It is respectfully submitted that this rejection is in error and should be withdrawn. More specifically, as far as can be determined, the Office Action appears to base the rejection on the basis that the claims specify that only a *portion* of the received address is used for comparison, whereas the specification of the present application uses all of a received address (rather than just a portion of it) for the comparison. This is incorrect. A full address specifies both a chip and a location on the specified chip: it is the portion of the full address specifying the chip that is "portion of the received address" compared in the claims. Further, even for this chip-specifying 5-bit (in the example) portion, there present application presents embodiments where enabling/disabling is based on only a sub-portion of this 5-bit portion of an entire address.

In more detail, as described in detail in the present application, an address includes both an address *of* a particular chip and of a location *on* that particular chip. See, for example, at lines 6-9 of paragraph [0091], where the emphasis is added:

> The sequencer 543 first shifts out the select address for selecting a *particular memory device chip* 141, *followed by an address of a memory chunk* (e.g. 64 bits) from the address control registers through the lines 551 via the MUX/SERDES 519 to the serial-in lines SI0, SI1.

See also, for example, the description of paragraph [0075] on the address shift register 333 its use for supplying the address on the chip to the 18-bit address bus internal to the chip. Of the entire address, consisting of the array address and the address on the array, it is only this first portion of a received address, the (here) 5-bit array address, that is compared with the first and second codes. (Note also, as described at paragraph [0049], the use of five bits to specify an array address is just one particular embodiment.)

Further, as noted in paragraph [0071], in the exemplary process of chip selection, it is actually *6*-bits of address that are loaded into a shift register, but only a *5*-bit portion of these six bits that is compared. At lines 3-5, paragraph [0071] reads, with added emphasis, as:

> After three P/D* clock periods, ***6*** bits have been loaded into the shift register 301 and *only the least significant 5 bits are used by the comparator 303.*

Thus, again, only a portion of the received address is compared.

Additionally, the present application also presents embodiments where only a part of the array address portion of the address is compared to enable or disable a memory chip; that

is, a sub-portion of a portion of the received address is used for the comparison. Such embodiments are described briefly at lines 3-6 of paragraph [0019]:

> The multi-bit address in the multi-bit mount for each memory device is partitioned into two subsets. The permutations of one subset are used to provide the different memory-device addresses on a memory module.

These embodiments are developed further with respect to figure 2B and its description at in paragraphs [0051] and [0052] and elsewhere. Thus, as described at line 4 of paragraph [0052]: "only a subset of the bits of the multi-pin mount is required." And in the last sentence of paragraph [0052]:

> For a 5-bit mount, two of the bits are configured for four memory-device addresses on each memory sub-module ...

Thus only two of the five bits of the device address are used for a comparison to enable/disable a memory chip on each sub-module.

Thus, the 5-bit address to which the Office Action refers is itself only a portion of the received address. Further, these five bits are only a portion of the address that is latched for comparison to enable/disable a chip. Additionally, for this array address (which itself is only a portion of the received address), embodiments are presented which use only a sub-portion of this portion for comparison. Consequently, for any of these reasons, it is believed that the Office Action's rejection of claims 40-54 under 35 U.S.C. 112, first paragraph, is incorrect and should be withdrawn.

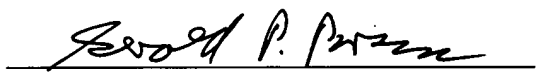
The Office Action also rejected claims 40-54 under 35 U.S.C. 135(b). This is also respectfully submitted to incorrect. The Office Action rejects these claims as not being made prior to one year from the date on which Pub. No. US 2002/0052633 was published. The Office Action appears to be incorrectly applying 35 U.S.C. 135(b)(2) here, when instead 35 U.S.C. 135(b)(1) is appropriate. Claims 40-54 of the present application are respectively exact copies of claims 1-15 of US patent 6,525,986. *These claims are not found in Pub. No. US 2002/0052633.* A review of the file history of US patent 6,525,986 shows that claims 1-15 of this patent were added by a supplemental preliminary amendment filed on July 10, 2001, were not part of the original application, and due not appear in the version of this application published as Pub. No. US 2002/0052633. Consequently, the provisions of 35 U.S.C. 135(b)(1) apply here, not 35 U.S.C. 135(b)(1). US patent 6,525,986 issued on February 25, 2003; claims 40-54 of the present application, which are respectively exact copies of claims 1-15 of US patent 6,525,986, where copied into the present application by

preliminary amendment on February 23, 2004. Consequently, the requirements of 35 U.S.C. 135(b) are met.

Considering the comments of paragraph 4 on page 3 of the Office Action, these are also believed to be error. Claims 40-54 of the present application are respectively exact copies of claims 1-15 of US patent 6,525,986 and are believed to be directed to the same invention as described within 37 CFR 41.201. It is again requested that an interference be declared.

For the above stated reasons, it believed that the Office Action's rejections of the pending claims are in error and that the claims are allowable in the present application. A prompt declaration of the requested interference is respectfully requested. In the meantime, however, if the Examiner has any questions about this request, application or disclosure statements, a telephone call to the undersigned is invited.

Respectfully submitted,



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